



# Xilinx<sup>®</sup> Spartan<sup>™</sup> -3E Evaluation Kit User Manual

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## 1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Spartan-3E Evaluation Kit from Avnet Design Services. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the example projects.

### 1.1 Description

The Spartan-3E Evaluation Kit provides a platform for engineers designing with the Xilinx Spartan-3E FPGA. The board provides the necessary hardware to not only evaluate the features of the Spartan 3E but also to implement user applications with a basic set of peripherals. Example projects are provided to help the user understand the design tool flow and leverage from known functional designs.

### 1.2 Features

#### **FPGA**

- Xilinx XC3S100E-TQ144 Spartan-3E FPGA

#### **Board I/O Connectors**

- 50-pin header for user I/O
- 8 discrete LEDs
- 2 push-buttons
- 4-position DIP-switch
- Dual character alpha numeric display

#### **Memory**

- ST Microelectronics SPI serial FLASH

#### **Communication**

- USB 2.0
- RS-232 serial port

#### **Power**

- USB or 5V wall-mount (not included)
- Texas Instruments TPS75003 triple supply

#### **Configuration**

- SPI serial FLASH to FPGA
- USB download utility
- Support for Xilinx Parallel Cable IV
- Fly-wire support for and Xilinx or compatible cable

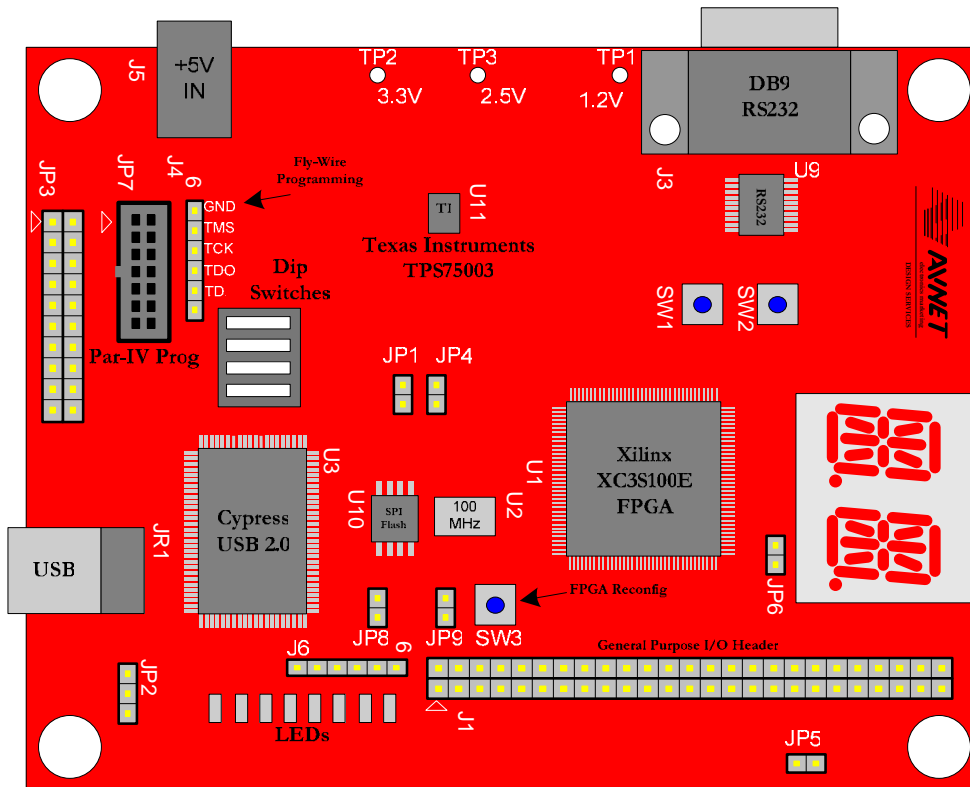


Figure 1 - Virtex-4 FX Evaluation Board Picture

### 1.3 Demo Applications

The Spartan-3E Evaluation Kit from Avnet Design Services comes with example projects designed in Xilinx ISE. The example projects help the user get started by leveraging already tested and functional designs. The example projects that will be discussed in detail later in this document are listed below.

\*Note: There may be additional demos which were developed after the printing of this document. For additional demo applications, please contact your local Avnet FAE.

#### Segment Test Project

- Display count value on segment display
- Provide test message over RS232
- Source Code Included

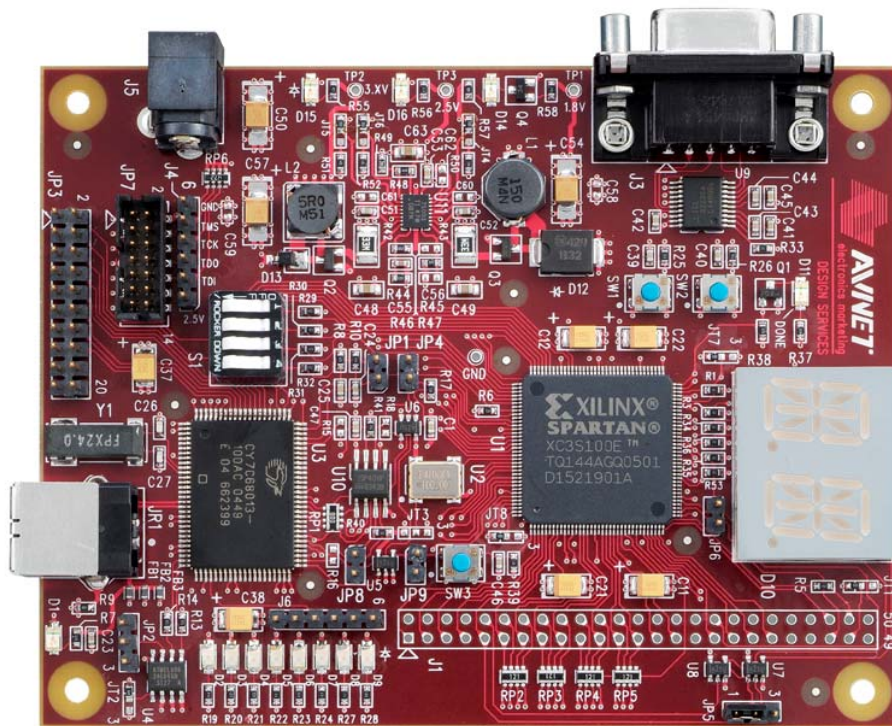


Figure 2 - Spartan-3E Evaluation Board Picture

## 1.4 Ordering Information

The following table lists the evaluation kit part numbers and available software options.

For more information, visit the Internet link at <http://www.em.avnet.com/ads> or [www.em.avnet.com/spartan3e-evl](http://www.em.avnet.com/spartan3e-evl)

Part Number	Hardware
ADS-XLX-SP3E-EVL100	Xilinx Spartan-3E Evaluation Kit with an XC3S100E
ADS-BASEX-BUNDLE	ISE BaseX (only available with purchase of the above part number)

Table 1 - Ordering Information

## 2.0 Hardware

This section of the manual describes the hardware of the Spartan-3E Evaluation Board. The hardware was designed with the Spartan-3E FPGA as the focal point. The block diagram is shown in Figure 8.

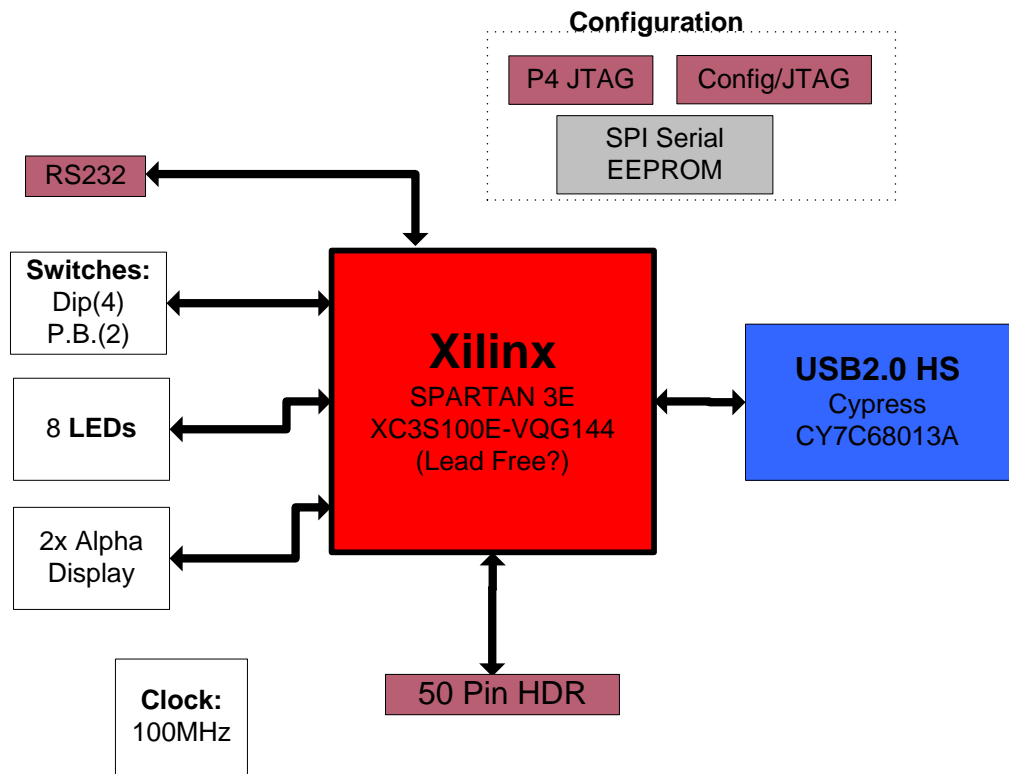


Figure 3 - Spartan-3E Evaluation Kit Block Diagram

### 2.1 Spartan-3E FPGA







The Spartan-3E Evaluation Board was designed to support the Spartan-3E FPGA in the 144-pin package (TQ144). This package supports two densities 3S100E and 3S250E though initially only the 3S100E will be offered in a product. Table 2 describes the attributes of the Spartan-3E device based on density.

Spartan-3E Part	System Gates	Logic Cells	BlockRAM (bits)	BRAM	Dedicated Multipliers	DCMs	Max User I/O (144 package)
XC3S100E	100K	2,160	72K	4	4	2	108
XC3S250E	250K	5,508	216K	12	12	4	108

Table 2 - Spartan-3E Attributes by Density

## 2.2 Configuration

The Spartan-3E Evaluation Board supports Boundary-scan (JTAG) and SPI programming methods. In addition, the user may use the Avnet USB utility to configure the FPGA and/or SPI flash device.

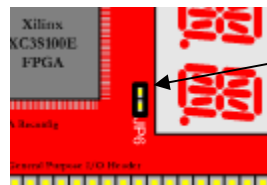
Configuration Mode (M2 : M1 : M0)	USB CCLK En JP4	Mode Select JP6	Notes
SPI <b>DEFAULT</b> (0:0:1)	 JP4	 JP6	<b>DEFAULT</b> FPGA provides SPI protocol to read from the Flash.
Boundary Scan (1:0:1)	 JP4	 JP6	FPGA will <b>not</b> attempt configuration over SPI or other means. It may be programmed directly over the JTAG interface.
USB (NA)	 JP4	 JP6	In this mode the FPGA is configured over USB from a Host PC. A Windows utility is provided.

**Table 3 - FPGA Configuration from PROM/JTAG ... Jumper Setting**

### 2.2.1 Boundary Scan

Programming the Spartan-3E FPGA via Boundary-scan requires a JTAG download cable (not included in the kit). The Spartan-3E Evaluation Board has connectors to support both the flying leads connection of the Parallel Cable III and the ribbon cable connection of the Parallel Cable IV. These connectors are labeled “J4” and “JP7” respectively.

When programming the FPGA via the JTAG interface, it is good practice to place the device in Boundary Scan mode. This may be accomplished using the Mode select jumper JP6. With JP6 off, the mode pins M[2:0] will be 001 which enables SPI programming mode. With JP6 installed, the mode pins M[2:0] will be 101 which enables boundary scan mode. Note that power should be removed when changing the programming Mode.



For Boundary Scan mode, place a jumper at JP6

**Figure 4 - Boundary Scan Mode Selection via JP6**

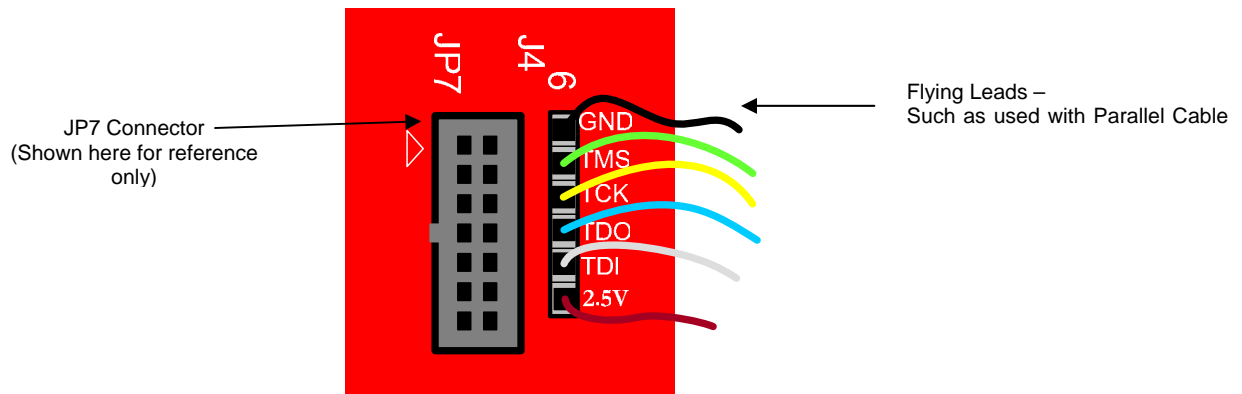
### JTAG Header (J4)

J4 is a 6x1 standard 0.1” header and is intended for use with flying leads, such as those of the Xilinx Parallel Cable 3 (PC3) downloading/debugging cable. Connect the leads as indicated in Table 4 below for “J4” as demonstrated in Figure 5.

Signal Name	Par-3 (J4) pin	PAR-4 Ribbon (JP7) pin
VCC	1	2
TDI	2	10
TDO	3	8
TMS	5	4
TCK	4	6
GND	6	1,3,5,7,9,11 or 13

**Table 4 - JTAG Headers (Par-3 & Par-4) Pin-Out**

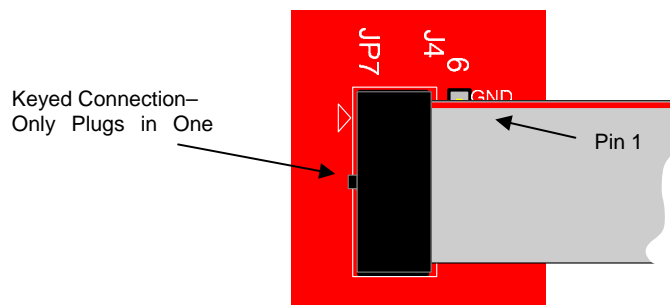




**Figure 5 - Configuration Connections – Par3**

#### **Parallel Cable IV / MultiPro Ribbon (JP7)**

JP7 is intended for connection to a 14-pin ribbon as supplied with a Xilinx Parallel Cable IV or MultiPro Desktop Tool. Connect the ribbon cable to JP7 as shown below. Note that the ribbon and connector are keyed to ensure proper installation.



**Figure 6 - Configuration Connections – Par IV**

For further information regarding Xilinx configuration solutions, please visit:

[http://www.xilinx.com/products/design\\_resources/config\\_sol/index.htm](http://www.xilinx.com/products/design_resources/config_sol/index.htm)

#### **2.2.2 Configuring FPGA with SPI FLASH (default)**

When the configuration mode is set to SPI the Spartan3E will attempt to configure after power up by sequentially loading data from the SPI FLASH starting at address 0x0. SPI mode is selected by removing the jumper at JP6 which is the factory default.

The SPI FLASH is programmed via the methods discussed in section 2.4 of this manual using a HEX file as generated according to the instructions in section 2.3.

#### **2.2.3 Configuring FPGA over USB**

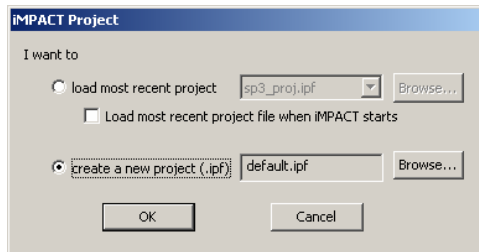
The FPGA pins required for configuration are attached to the CY68013 USB controller allowing a host controller to initialize the Spartan3E FPGA and download a new .BIT configuration file. This kit includes a Windows utility for configuration and programming over USB. These functions are not supported by Avnet on other platforms but source code is included as a reference for customers who want to add it. The operation of the utility is described in section 2.5 of this manual.

## 2.3 Creating a .HEX file

Configuration via SPI requires that a .HEX file be generated from a working .BIT configuration file. Due to the time and complexity involved with creating this file and programming the SPI FLASH device it is recommended that the .BIT file be tested prior to committing it to FLASH.

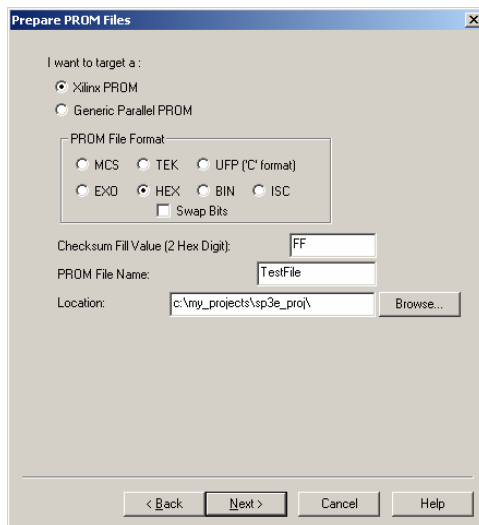
NOTE: When creating the HEX file, be sure to use a BIT which was generated with the startup clock option set for CCLK (typically the default).

The screen shots that follow show the step by step procedures of creating a .HEX file using iMPACT 7.1. This procedure may need to be modified when using a different version of the tool.



Immediately after opening iMPACT it is necessary to either select a preexisting project or create a new one. This process assumes that a new project will be created. The project can be saved after completing the process to save steps on subsequent passes.

In the next 2 screens select "Prepare Configuration Files" and "PROM File" and clicking "Next" after each.

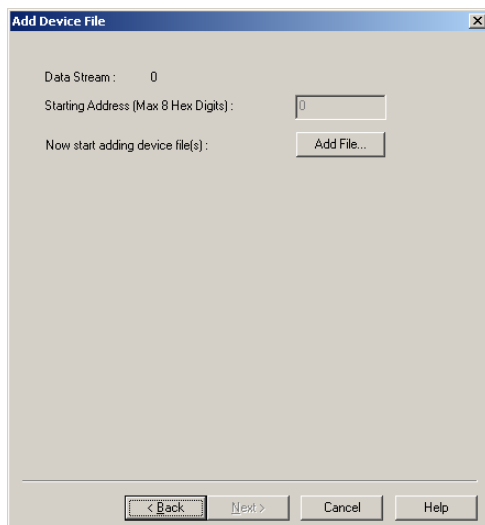


The following screen shown at the left is where the properties of the file to be generated are set. Even though the SPI PROM on the board is not manufactured by Xilinx, select "Xilinx PROM" as the target and "HEX" for the format.

The Checksum Fill Value is the expected value in FLASH after it has been erased, "FF" for this device.

The "PROM File Name" is the name of the file to be generated (.HEX will be added by the tool) and location is the path to where it is to be saved. These can be any valid windows expressions but avoid spaces as the Xilinx tools sometime have trouble with spaces in file names and pathways.

In the next window check "Auto Select PROM" and then next twice.



The next step is to add the .BIT file to be converted.

### \*\* NOTE \*\*

The BIT file must be created with CCLK selected as the start up clock or the resulting HEX file will not configure the FPGA.

Multiple file are not supported so select NO when asked if a second file is to be added.

Then "Finish" and "Yes" to generate the file.

## 2.4 Programming SPI FLASH

An FPGA configuration file should first be tested by programming the BIT format directly into the FPGA via boundary scan. See the appropriate section of this document for boundary scan (JTAG) programming. When a bit file has been tested to the point where it is ready for non-volatile storage, iMPACT should be used to convert the BIT to a HEX format as described in Section 2.3. When creating the HEX file, be sure to use a BIT which was generated with the startup clock option set for CCLK (typically the default).

The primary purpose of the SPI FLASH on this board is to store the configuration file for the FPGA but the unused portion of the FLASH, or the entire FLASH if an alternate configuration method is used, can be used to store user data or code require by the FPGA application.

The programming methods below can be used to write configuration and/or data to the device.

### \*\* NOTE\*\*

JP8 provides write protection for the SPI FLASH device so this shunt must be removed before programming.

### External Programming

There are many programmers on the market which are capable of programming the SPI device. To program the device with this method, it would likely require the device be removed from the PCB. While external programming may be ideal for a production environment prior to mounting the components, it is obviously not for development. Thus a method of in-circuit programming is desirable.

### In-Circuit Programming

In-Circuit programming of the SPI FLASH can be accomplished on this board from a host PCI via USB with the provided utility or with an external controller via the interface provided by the header "J6".

#### Programming via USB

The Avnet USB utility may be used to write data to the SPI Flash device. The Avnet USB utility will accept a HEX file as an input and program it into the SPI Flash. The HEX is actually an ASCII file, so there is a conversion going on in the background which is transparent to the user. For additional information on the Avnet USB utility, please see the included documentation.

#### Programming with J6

The SPI Flash pins have been made available at J6. This will allow the user to program the part via an external custom method. It may be necessary when programming the SPI in this mode to place a shunt on JP9 to hold the Spartan3E PROG# pin low tri-stating the FPGA pins to avoid contention on the programming signals. The pinout for J6 is given in the following table.

J6 pin	Net name	SPI Function	FPGA Pin
1	VCC (3.3V)	VCC	-
2	FPGA_CS#	CS#	P39
3	DIN	MISO	P63
5	FPGA_CCLK	CLK	P71
4	FPGA_MOSI	MOSI	P44
6	GND	GND	-

**Table 5 - J6 Header (SPI) Pin-out**

This method of programming is allowed but it is not supported by Avnet.

#### Programming with FPGA

Since the configuration pins of the FPGA are available as I/O, the user could create IP to read/write the SPI Flash. At the time of this publication, an example project for doing so was not available. The task of creating such a project is left to the user. Check with your local Avnet FAE to see if such projects or cores are currently available through Avnet or Xilinx.

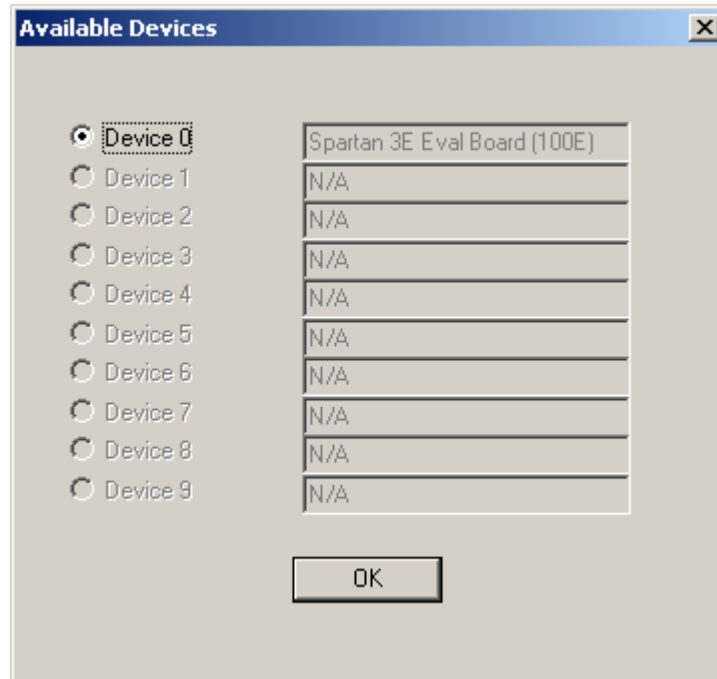
## 2.5 Avnet USB Utility

The Avnet USB Utility may be used to configure the FPGA and program the SPI Flash memory as mentioned in the previous section. This section will describe the basic operation of the Avnet USB utility; more detailed information is available in the utility user manual. Whether configuring the FPGA or programming the FLASH make sure that the BIT file is configured with the startup clock set to CCLK and that there is a shunt on JP4 enabling the USB controller to drive the CCLK signal.

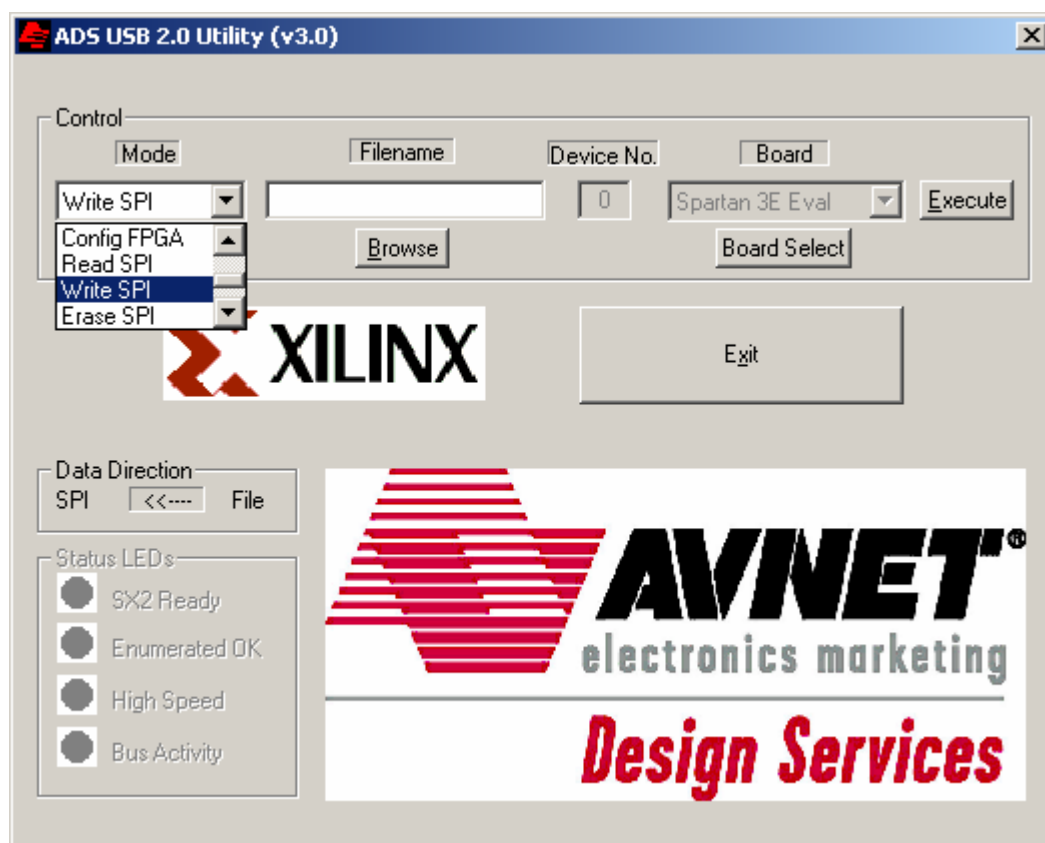


The following instructions and screen shot are an overview of the procedure. They assume that the driver and utility version 3.0 or later has been properly installed. Consult the USB Utility User Manual as needed for this procedure.

1. Connect a USB cable from the host PC to the Spartan3E Eval board.  
**Note:** The board will draw it's power from the USB port, so there is no need to apply power to the optional barrel power input.
2. **Wait!** It will take a few seconds to scan the USB bus and show the available Avnet Boards
3. Select "Spartan 3E Eval" in the "Board" drop down menu.
4. Select the desired mode from the "Mode" drop-down menu.
5. Browse to or enter a filename appropriate for the selected mode.
  - a. "ConfigFPGA" requires a .BIT file
  - b. "Write SPI" (Configuration) requires a .HEX file and must start at address "00000"For other options reference the Utility User Guide
6. Click the "Execute" button, the operation doesn't start until this button is selected.
7. **Wait!** After a few seconds a progress bar will track the progress.
8. A window will pop up when the process completes or if it errors out.



**Figure 7 - Select Target Board**



**Figure 8 - USB Utility GUI**

## 2.6 Jumper Settings

This section provides a description of the jumper settings for the Evaluation Board. The jumpers are listed in order by JP number. The board is ready to use out of the box with the default jumper settings.

**JP1 “USB RESET”** – Jumper installed forces Cypress USB device into reset.

**JP2 “USB EEPROM WC#”** – Serial EEPROM write protect, install a shunt at position 1-2 to protect data in the upper quadrant. For normal operation, leave shunts off or place at position 2-3. Pin is internally pulled low.  
Default: Open, read/write enabled.

**JP3 “USB EEPROM Unused Pins”** – JP3 is actually a 10x2 header which allows user access to the Cypress EZUSBFX2 part which are not otherwise connected on this board.

**JP4 “USB CCLK ENABLE”** – USB CCLK Enable, when installed enables the USB device to drive the configuration clock of the FPGA.  
Default: Open, the FPGA provides the configuration clock.

**JP5 “Display Enable”** – Jumper position 1-2 to enable the 2 character led segment display.

**JP6 “Force JTAG Mode”** – Use this jumper to enable JTAG mode. When installed, FPGA is in boundary scan mode. When uninstalled, the FPGA will be in SPI mode.



JP7 "JTAG Par – IV" – This is actually a connector. Use this connector when programming the device over JTAG with a ribbon, as used with the Xilinx Parallel IV cable.

JP8 "SPI Flash WP" – A jumper on JP8 forces the device's WP# signal low, and places the device in write protect mode. For normal operation (writes enabled) leave this jumper uninstalled.

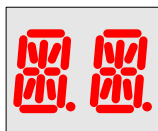
JP9 "FPGA Prog" – A jumper at this position will force the FPGA Prog# signal low. This jumper may be used to place the FPGA's pins in tri-state condition. Note that if HSWAP is enabled, the FPGA will have internal pull-ups on the pins.



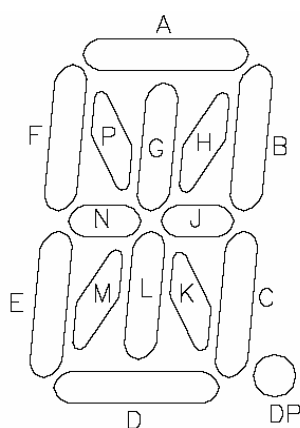
## 2.8 On-board Display (2 Character Alphanumeric LED)

Manufacturer: Lite-On

Part #: LTP-3786E-03



The Spartan-3E Evaluation board uses a dual digit 14-segment alphanumeric display from Lite-On. To enable the display, place a jumper at JP5 position 1-2. Each segment may be controlled by the FPGA General Purpose I/O bus as listed below. The GEN\_IO 9 and 10 nets are used to drive the segment anodes, while a logic low on GEN\_IO11-25 enables the individual segments.



Display Pin#	Display Pin Name	FPGA Pin#	GEN_IO#
11	Char2 Anode	P7	9
16	Char1 Anode	P91	10
8	DP	P8	11
17	P	P88	12
13	N	P14	13
2	M	P87	14
4	L	P15	15
5	K	P86	16
6	J	P16	17
14	H	P82	18
15	G	P26	19
18	F	P85	20
1	E	P20	21
7	D	P83	22
9	C	P21	23
10	B	P81	24
12	A	P22	25

Table 7 - Ethernet PHY Modes

## 2.9 DIP & Push-button Switches

A four-position dipswitch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low (0) by 4.7K ohm resistors when the switch is open and tied to 3.3V (1) when the switch is closed.

Switch #	Signal Name	FPGA pin#
S1-1	SWITCH0	P107
S1-2	SWITCH1	P111
S1-3	SWITCH2	P114
S1-4	SWITCH3	P119

Table 8 - DIP switch FPGA Pin-out



Two momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low (0) until the switch closure pulls it high (1).

Silkscreen Part #	Signal Name	FPGA pin#
SW1	SWITCH_PB1	P69
SW2	SWITCH_PB2	P66

**Table 9 - Push button FPGA Pin-out**

## 2.10 LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is Low (0). These pins are shared with the General Purpose bus as indicated below.

LED #	Signal Name	FPGA pin#
D2	GEN_IO_1	P2
D3	GEN_IO_2	P96
D4	GEN_IO_3	P3
D5	GEN_IO_4	P94
D6	GEN_IO_5	P4
D7	GEN_IO_6	P93
D8	GEN_IO_7	P5
D9	GEN_IO_8	P92

**Table 10 - LED FPGA Pin-out**

## 2.11 Memory

The Spartan-3E Evaluation Board is populated with a 4Mbit low voltage serial flash memory from ST Microelectronics. This memory may be used to configure the S3E FPGA or to store user data.

### 2.11.1 SPI Flash

Manufacturer: ST Microelectronics  
Part #: M25P40-VMN6P

Attributes of the Serial Flash memory:

- 4Mbit
- Up to 40MHz SPI compatible serial interface
- 2.7V to 3.6V operation

Since the FPGA programming pins are available to the user after configuration, it is possible to use memory for external data storage. The following table illustrates the pin-outs of the FPGA to SPI flash memory.

SPI Flash Pin#	SPI Flash Pin Name	FPGA Signal Name	FPGA pin#
1	S#	FPGA_CS#	P39
2	Q	DIN(MISO)	P63
3	W#	-	-
7	Hold#	-	-
6	C	FPGA_CCLK	P71
5	D	FPGA_MOSI	P44

**Table 11 - SPI FPGA Pin-out**

Please see also the configuration section of this document for information on configuring the FPGA with SPI.

### \*\* NOTE\*\*

JP8 provides write protection for the SPI FLASH device so this shunt must be removed before programming.

## 2.12 Communication (RS-232, USB 2.0)

For communication, the Spartan-3E FPGA has access to an RS232 transceiver and a USB2.0 transceiver.

### 2.12.1 RS-232

Manufacturer: Harris/Intersil  
Part #: ICL3222CA

The RS232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver is operating at 3.3V for VCC. The internal charge pump creates the RS232 compatible output levels.

The standard RX and TX lines (pin3 and pin2) are connected to the FPGA by way of the 3222. Please see the table below for the FPGA pinout.

A straight through serial cable should be used to plug "J3" into a standard PC serial port (male DB9).

Signal Name	FPGA pin#	Xcvr pin#	Note (from FPGA perspective)
Transmit (RS232_TX1)	P67	13	Out to DB9-2
Receive (RS232_RX1)	P47	15	In from DB9-3
CTS (RS232_CTS)	P68	12	Out to DB9-8
RTS (RS232_RTS)	P48	10	In from DB9-7

Table 12 - RS-232 FPGA Pin-out

Signal Name	DB9 J3	Xcvr pin#
TX	2	17
RX	3	16
CTS	8	8
RTS	7	9
GND	5	-

Table 13 - RS-232 Connector Pin-out

### 2.12.2 USB 2.0

Manufacturer: Cypress  
Part #: CY7C68013-100AC

The Spartan-3E Evaluation Board includes a Cypress EZ-USB FX2™ USB Microcontroller, part number CY7C68013-100AC. The EZ-USB FX2 device is a single-chip integrated USB 2.0 transceiver, Serial Interface Engine (SIE) and 8051 microcontroller. This device supports full-speed (12 Mbps) and high-speed (480 Mbps) modes, but does not support low-speed mode (1.5 Mbps). The FX2 interface to the Spartan-3E FPGA is a programmable state machine that supports 8- or 16-bit parallel data transfers. This interface is called the General Programmable Interface (GPIF). The GPIF is controlled by Waveform Descriptors that are created with the Cypress "GPIFTool" utility and downloaded to the FX2 over the USB cable. The GPIF descriptors are stored in internal RAM and are loaded by the firmware during initialization. The GPIF interface is made up of the signals in the following table, which are connected to Spartan-3E FPGA.

Some of the additional GPIF pins are connected to the configuration port on the Spartan-3E FPGA. This provides for the development of a FPGA configuration tool, which may be created by Avnet at a later date. The pins which will affect FPGA configuration are shaded in the following table.

The USB FX2 device can also be used in a slave mode where the FPGA accesses the FX2 like a FIFO. For more information about the FX2 modes of operation, see the "EZ-USB FX2 Technical Reference Manual" and the FX2 datasheet available on Cypress Semiconductor's web site (<http://www.cypress.com>).

FX2 Signal	Board net name	FPGA pin	Description
CTL[0]	USB_CTL0	P141	Programmable control outputs
CTL[1]	USB_CTL1	P136	
CTL[2]	USB_CTL2	P120	
CTL[3]	CTL3_PROG#	-	Output enable for FPGA_PROG# driver. <b>A low on this pin will drive the FPGA_PROG net.</b>
CTL[4]	CTL4_IFC_EN	-	Allows FX2 to drive the FPGA CCLK see schematic pg4. Requires R16. *Formerly connected to FPGA CS# on other Avnet Boards. <b>Affected by JP4, GPIFADR[0], and IFCLK</b>
CTL[5]	FPGA_RDWR#	P56	SelectMAP port read/write enable. Requires R15.
RDY[0]	USB_RDY0	P139	Sample-able ready inputs
RDY[1]	USB_RDY1	P140	
RDY[2]	FPGA_BUSY	P43	
RDY[3]	FPGA_DONE	P72	FPGA configuration DONE pin
RDY[4]	FPGA_INIT#	P40	FPGA initialization pin
RDY[5]	USB_RDY5	-	Sample-able ready input connected to JP3:15 Bidirectional FIFO data bus (also SMAP data) <b>FD0 connected to USB pins 34 and 62(DIN). FD1&amp;FD2 determined by JT10&amp;JT12.</b>
FD[0]	USB_FD0	P63	
FD[1]	USB_FD1	P59, P62	
FD[2]	USB_FD2	P58, P60	
FD[3]	USB_FD3	P54	
FD[4]	USB_FD4	P53	
FD[5]	USB_FD5	P52	
FD[6]	USB_FD6	P51	
FD[7]	USB_FD7	P50	
FD[8]	USB_FD8	P113	
FD[9]	USB_FD9	P112	Bidirectional FIFO data bus
FD[10]	USB_FD10	P106	
FD[11]	USB_FD11	P105	
FD[12]	USB_FD12	P104	
FD[13]	USB_FD13	P103	
FD[14]	USB_FD14	P98	
FD[15]	USB_FD15	P97	
GPIFADR[0]	USB_PC0	P71	Optional FPGA_CCLK out – See schematic sheet 4. <b>Affected by JP4, CTL4_IFC_EN, and IFCLK</b>
GPIFADR[1]	FPGA_M2	P57	SelectMAP port mode - M2
GPIFADR[2]	FPGA_M1	P58, P60	SelectMAP port mode - M1 <b>Connection determined by JT11.</b>
GPIFADR[3]	FPGA_M0	P59, P62	SelectMAP port mode - M0 <b>Connection determined by JT9.</b>
GPIFADR[4]	FPGA_MOSI	P44	FPGA Master Out Slave In (input to SPI Flash). May be used to write data to SPI.
GPIFADR[5]	DIN(MISO)	P63	Programming input to FPGA (Data out from SPI Flash). May be used to program FPGA or read data from SPI. <b>Also connected to USB_FD0.</b>
GPIFADR[6]	FPGA_CS#	P39	CS pin for SPI Flash Part
GPIFADR[7]	-	-	No Connect
GPIFADR[8]	USB_PE7	-	Address output connected to JP3:16
IFCLK	USB_IFCLK	P126	Interface clock
PA0/INT0#	USB_INT0#	P135	Port A I/O or active-low interrupt 0
PA1/INT1#	USB_INT1#	P134	Port A I/O or active-low interrupt 1
PA2/SLOE	USB_SLOE	P125	Port A I/O or slave-FIFO output enable
PA3/WU2	USB_WU2	P124	Port A I/O or alternate wake-up pin
PA4/FIFOADR0	USB_FA0	P123	Port A I/O or slave-FIFO address select 0
PA5/FIFOADR1	USB_FA1	P122	Port A I/O or slave-FIFO address select 1
PA6/PKTEND	USB_PEND	P117	Port A I/O or slave-FIFO packet end

FX2 Signal	Board net name	FPGA pin	Description
PA7/SLCS#	USB_SLCS#	P116	Port A I/O or slave-FIFO enable
RESET#	USB_RESET#	-	Not connected to FPGA. May use JP1 to force USB device active-low reset
CLKOUT	USB_CLKOUT	P128	Clock output from USB
SCL	SCL	-	Serial prom clock
SDA	SDA	-	Serial prom data
WAKEUP#	USB_WAKEUP#	-	USB wakeup signal
RXD0	USB_UART_RX0	P131	USB UART Receive
TXD0	USB_UART_TX0	P130	USB UART Transmit
RXD1	USB_RXD1	-	JP3, PIN1
TXD1	USBTXD1	-	JP3, PIN3
INT4	USB_INT4	-	JP3, PIN5
INT5#	USB_INT5#	-	JP3, PIN7
TIMER2	USB_TIMER2	-	JP3, PIN9
TIMER1	USB_TIMER1	-	JP3, PIN11
TIMER0	USB_TIMER0	-	JP3, PIN13
PE0	USB_PE0	-	JP3, PIN2
PE1	USB_PE1	-	JP3, PIN4
PE2	USB_PE2	-	JP3, PIN6
PE3	USB_PE3	-	JP3, PIN8
PE4	USB_PE4	-	JP3, PIN10
PE5	USB_PE5	-	JP3, PIN12
PE6	USB_PE6	-	JP3, PIN14
PE7	USB_PE7	-	JP3, PIN16
WR#	USB_WR#	-	JP3, PIN19
RD#	USB_RD#	-	JP3, PIN18
BKPT	USB_BKPT	-	JP3, PIN17

**Table 14 - USB Interface FPGA Pin-out**

## 2.13 I/O Connectors

The Spartan-3E Evaluation Board may be populated with a 50-pin (2x25) header for access to I/Os.

### 2.13.1 Header “J1”

The 50-pin header labeled “J1” on the Spartan-3E Evaluation Board is connected to 47 I/O pins on the Spartan-3E FPGA. Pin 48 on the header provides either 3.3V or 5.0V depending on the jumper pad installation on JT9 (3.3V is the default). Note that the pins of header JP1 are shared with several other peripherals including LEDs and LED segment display. Please see the schematic and/or other sections of this document for details.

The following table shows the pin-out for the header connector.

J1: Header 25x2					
Pin	FPGA	Signal	Signal	FPGA	Pin
2	P96	GEN_IO2	GEN_IO1	P2	1
4	P94	GEN_IO4	GEN_IO3	P3	3
6	P93	GEN_IO6	GEN_IO5	P4	5
8	P92	GEN_IO8	GEN_IO7	P5	7
10	P91	GEN_IO10	GEN_IO9	P7	9
12	P88	GEN_IO12	GEN_IO11	P8	11
14	P87	GEN_IO14	GEN_IO13	P14	13
16	P86	GEN_IO16	GEN_IO15	P15	15
18	P82	GEN_IO18	GEN_IO17	P16	17
20	P85	GEN_IO20	GEN_IO19	P26	19
22	P83	GEN_IO22	GEN_IO21	P20	21
24	P81	GEN_IO24	GEN_IO23	P21	23
26	P77	GEN_IO26	GEN_IO25	P22	25
28	P76	GEN_IO28	GEN_IO27	P23	27
30	P75	GEN_IO30	GEN_IO29	P25	29
32	P74	GEN_IO32	GEN_IO31	P10	31
34	P41	GEN_IO34	GEN_IO33	P32	33
36	P12	GEN_IO36	GEN_IO35	P33	35
38	P18	GEN_IO38	GEN_IO37	P34	37
40	P24	GEN_IO40	GEN_IO39	P35	39
42	P29	GEN_IO42	GEN_IO41	P132	41
44	P31	GEN_IO44	GEN_IO43	P142	43
46	P36	GEN_IO46	GEN_IO45	P38	45
48	P17	GEN_IO_CLK	3.3V/5.0V	-	47
50	-	Ground	Ground	-	49

**Table 15 - Header "J1" Pin-out**

## 2.14 Power

The Spartan-3E Evaluation Kit may be powered from an external 5V AC/DC Adapter (not supplied with the kit) or the USB interface.

### 2.14.1 External AC/DC Adapter "J5"

An AC/DC adapter is not provided with the kit. To power the board with an external supply, the user will provide +5V at the barrel connector labeled "J5". The barrel connector dimensions are given in the figure below. Note that the connection is center positive.

#### IMPORTANT:

Note that there is **no protection for reverse power supply polarity** so take necessary precautions to ensure that the center pin is +5V, and the ring is ground!

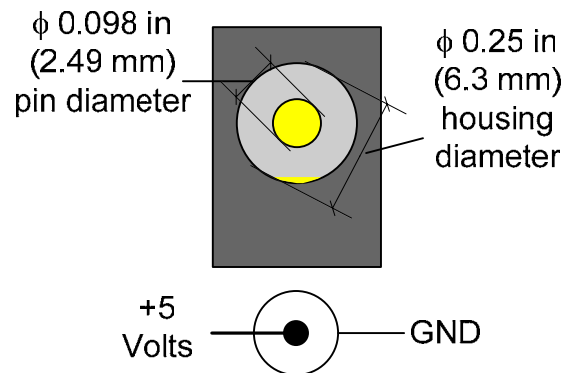


Figure 10 - Barrel Power Connector "J5"

### 2.14.2 USB Power

The Spartan-3E Evaluation kit may be powered from the USB port. To do so, use a standard USB cable plugged into a PC (or standard USB host) and plug the peripheral side of the cable in to JR1. This will supply +5V to the TI voltage regulator.

### 2.14.3 TI TPS75003

For voltage regulation, the Spartan-3E Evaluation kit uses a Texas Instruments TPS75003. This is a triple-supply power management IC, and is designed for use with FPGAs and ASICs. It features two 95% efficient buck regulators and an LDO. In this application, it uses the 5V input from the barrel or USB connectors to provide the 3.3V, 2.5V, and 1.2V required by the Spartan 3E device.

## 3.0 Software/BSP

This section of the manual describes the example projects included in the kit.

### 3.1 What is included

All of the example projects included in the Spartan-3E Evaluation Kit were created using the Xilinx Integrated Software Environment (ISE) 7.1.

- ISE Example Projects
  - Segment Test Project

#### 3.1.1 Segment Test Project

This example is intended to provide a test count on the segment display as well as blinking LEDs and a terminal output. The user may connect to the DB9 connector with a standard RS232 straight through (non-nullmodem) type cable. A terminal program (such as Hyperterm) may be used to view the output at 9600, 8, N, 1.



## 4.0 List of Partners

